AMENDMENTS TO THE SPECIFICATION:

Page 7, fourth paragraph, lines 6-7:

B1 cncl.

FIG. 9 is a view for explaining an operation of a ~~lamp~~ ramp system D/A converter circuit;

Page 13, first full paragraph, lines 6-8:

B2 cncl.

In the above mode of the invention, a ~~lamp~~ ramp type D/A converter circuit may be used as the D/A converter circuit. In that case, the number of the D/A converter circuits is not limited to k/n.

Page 18, last paragraph spanning page 18, line 24 to page 19, line 6:

B3 cncl.

In this embodiment, an example of a case where a ~~lamp~~ ramp system D/A converter circuit is adopted for a D/A converter circuit, will be described. FIG. 6 is a schematic view of a signal line driver circuit in the case where the ~~lamp~~ ramp system D/A converter circuit is used. Incidentally, also in this embodiment, although the description will be made on a case corresponding to the image display device of the XGA standard and a 3-bit digital picture signal, the present invention is not limited to the 3 bits, but is also effective for a case corresponding to another bit number or the image display device of a standard other than the XGA.

Page 20, first full paragraph, lines 7-21:

B4 cont

In order to explain the operation of the ~~lamp~~ ramp system D/A converter circuit in detail, FIG. 9 shows the operation timing of a period when one of the four signal lines is selected by the signal line selecting circuit. First, the RS-FF30 is set by the input of a set signal, and the output PW-i comes to have a Hi level. Next, the digital picture signal stored in the second latch circuit is compared with the count signals (C0 to C2) for every bit by exclusive-OR gates. In the case where all of the three bits are coincident, the outputs of all the exclusive-OR gates come to have the Hi level, and as a result, the output (inversion RC-i) of the 3-input NAND gate comes to have the Lo level (thus, RC-i comes to have the Hi level). The output of this 3-input NAND is also inputted to the RS-FF30, and when RC-i comes to have the Hi level, it is reset, and the output PW-i returns to the Lo level. FIG. 9 shows an output example of RC-i, PW-i, and DA-i in the case where the 3-bit digital picture signal {L-i(0), L-i(1), L-i(2)} is {0, 0, 1}. In this way, the

B4 cancel

information of the digital picture signal is converted into the pulse width of the output PW-i of the bit comparison pulse width converter circuit (BPC).

Page 21, second full paragraph, lines 9-12:

B5 cancel

As described above, in the present invention, the ~~lamp~~ ramp system D/A converter circuit can also be used as the D/A converter circuit, and about 1/4 of the related art is sufficient for the circuit structure, so that it becomes possible to greatly reduce the occupied area of the driver circuit and the number of elements.